European Commission

Information Society and Media Directorate – General

Overall SiP Cost Estimation

SmartCoDe

Project No.:	ICT-2009-247473
Deliverable No.:	D-3.1.1
Deliverable Title:	Overall SiP Cost Estimation
Due Date:	12-31-2010 (M12)

Nature:	Report
Dissemination Level:	Public
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Lead Beneficiary No.:	2
Lead Beneficiary:	IFAT

SmartCoDe has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013]) under grant agreement n° 247473

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1 Introduction

The SmartCoDe project is about

1) Developing new methods for automated energy management that specifically consider the requirements of Energy using Products (EuP) in homes / offices and local renewable energy providers such as information security and dependability.
2) Developing an inexpensive hardware/software implementation that can be integrated into arbitrary Energy using Products, providing them with the ability to communicate and to remotely control its use of power.
3) Demonstration of technical and economic feasibility and benefit of intelligent energy management in buildings and neighbourhoods

This report concentrates on hardware integration issues for a SmartCoDe wireless node, which is supposed to provide functionality for wireless communication and power metering&control of appliances with the aim to enable the application of demand side management and smart metering in private and small commercial buildings and neighbourhoods.

Nowadays purchasable modules are bulky and expensive. In order to address a new and potentially huge market in homes, business- and public buildings and offices these services must come for very little additional costs. Due to the number of hardware modules that need to be installed, one significant cost item of the total system costs (aside of maintenance-, operational- and service costs) are the hardware purchase and installation costs. While minimization of installation costs is addressed by providing a wireless communication interface, which even allows for retrofit without structural changes, for a successful future roll-out scenario one must additionally strive for cutting the hardware purchase costs down to an affordable level >for everyone<.

The SmartCoDe approach to cope with the latter issue is to extensively making use of highly integrated circuits and effective heterogeneous assembly-, packaging- and manufacturing technologies. The resulting small sized System-in-Package (SiP) also optimizes subsequent integration costs into all kinds of energy using appliances (Figure 1) due to its little space requirements.

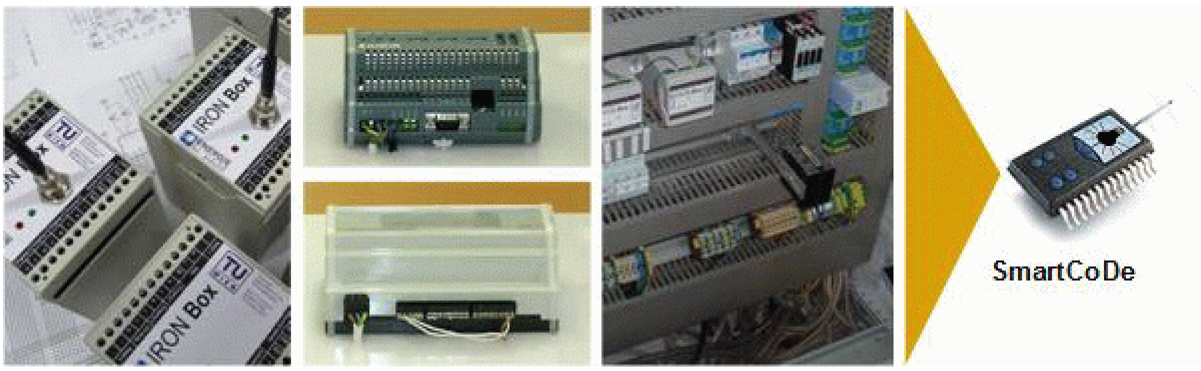

Figure 1: The vision of a SmartCoDe node

This report is organized in the following way:

Chapter 2 Internal Functions of a SmartCoDe Node sets the scope by presenting the functions to be provided by a SmartCoDe node.

Chaper 3 Architectures and Implementations discusses different implementations of (cost-) critical functions with their advantages and drawbacks.

Chapter 4 Overview of Appropriate Assembly- and Packaging Technologies gives an overview on assembly- and packaging technologies.

Chapter 5 SmartCoDe Node Cost Estimation finally comes up with a first cost estimation.

2 Internal Functions of a SmartCoDe Node

Figure 2 shows a functional block diagram of the targeted SmartCoDe node.

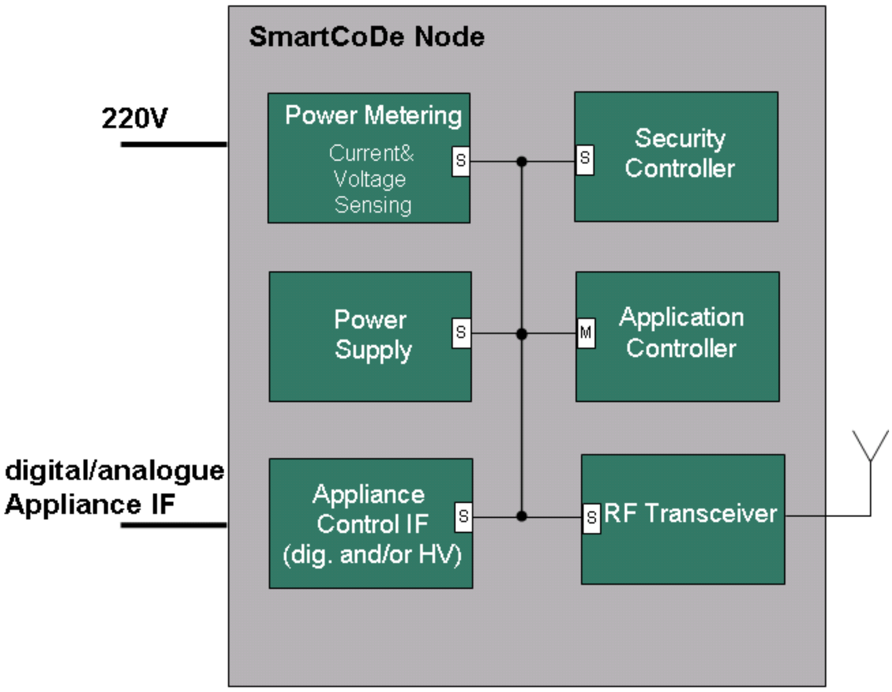

Figure 2: Functional Diagram of a SmartCoDe Node

From a functional point of view a SmartCoDe node consists of following main units:

- **Power Supply Unit**
  The Power Supply Unit is responsible for SmartCoDe node internal power supply. For that reason it must provide regulated DC voltage out of the 220V AC mains inputs for supplying SmartCoDe internal units. Due to the huge number of installed nodes, the Power Supply Unit must operate as energy-efficient as possible to not compromise overall energy consumption when the controlled appliance is turned off or in stand-by mode. It is assumed to be controllable by means of a digital bus slave interface by the Application Controller to enter different operational states for supporting different current-supply modes in order to increase energy efficiency.
- **Power Metering Unit**
  The Power Metering Unit is responsible for the measurement of the consumed (generated) power and energy of the corresponding energy using appliance (energy producing power generator) the node is integrated. By sensing the AC-voltage and current with appropriate sampling rate the consumed power can be calculated. The Power Metering Unit is considered to be an

autonomous slave device, regularly reporting the appliance-consumed power to the Application Controller via a digital bus interface.

- **Appliance Control Interface**
  The Appliance Control Interface is either analogue or digital. The analogue interface shall implement direct control of a power switch to turn simple electric loads on and off, e.g. for an "intelligent" power plug. For more complex appliances a simple digital, serial interface shall be provided. If the SmartCoDe node is only used for metering purposes, this interface can be omitted.
- **RF Transceiver**
  The RF Transceiver provides wireless control access. It integrates both wireless transmitting and receiving functions in order to both receive commands and report (power-) measurements or status information. The targeted carrier frequency is one of the license-free ISM-bands (ISM = Industrial, Scientific and Medical Band). The RF-Transceiver sends the received data to the Application Controller via a digital bus interface. On the other hand it wirelessly transmits data provided by the Application Controller at the same digital interface via the antenna.
- **Security Controller**
  For device authentification, binding and to protect sensitive information communicated via the wireless interface, dedicated security functionality supporting advanced cryptographic ciphering operations needs to be supported. Aside of encryption of data packets to be transmitted and decryption of secured received data packets this unit is also responsible for the associated key management. The Security Controller communicates with the Application Controller by means of a digital bus interface.
- **Application Controller**
  The Application Controller is a Microcontroller and is the central master unit within the node. It manages and controls all SmartCoDe node internal sub-functions and implements application specific functionality and the external wireless protocol.

3 Architectures and Implementations

The following chapter discusses architectures of sensitive functions to be implemented and co-integrated, thereby not only considering effects influencing functional complexity and performance, but also physical effects and countermeasures, that impacts the overall system-integration concept.

3.1 System Partitioning Issues

Internal functions of the SmartCoDe node impose certain constraints on their implementations to be considered. Particularly the necessity of signal processing in the 220V voltage domain (see Figure 3) has impact on chip partitioning, as cheap low feature sized CMOS technologies, which possesses high density integration (and therefore low area and low costs) cannot process directly such high voltages. Therefore this suggests a basic partitioning into low voltage signal processing ICs and high voltage signal processing ICs.

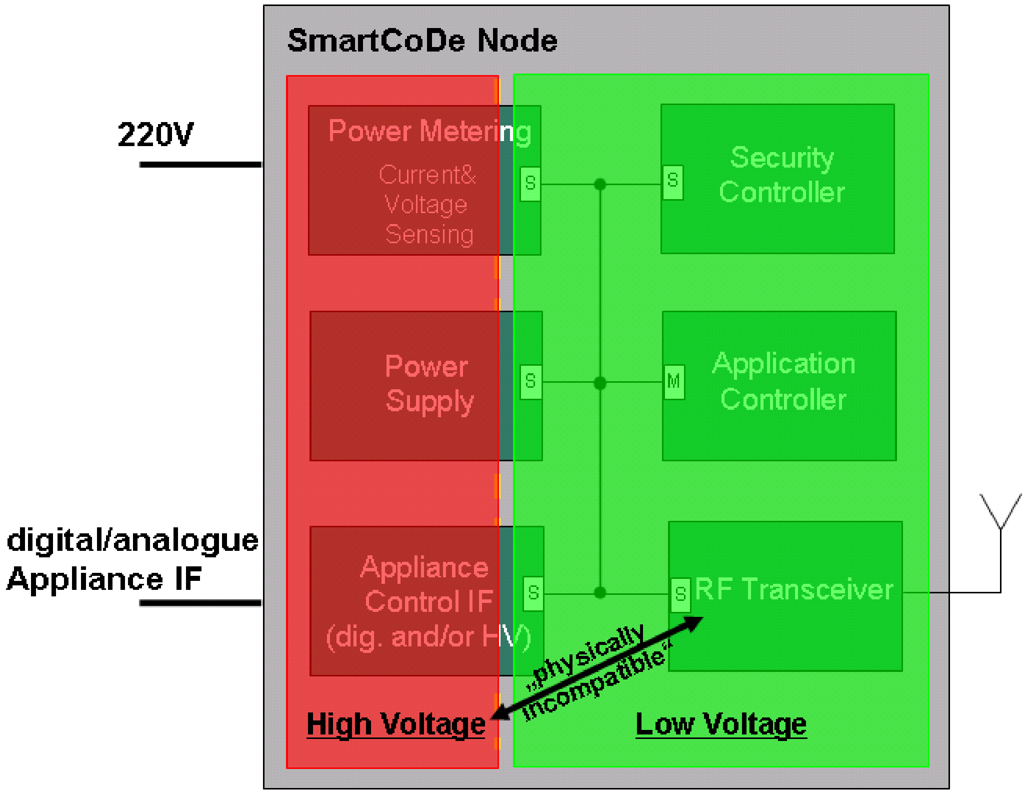

Figure 3: High/Low Voltage Domains of the SmartCoDe Node

Further on the RF module is quite sensitive to noise coupling and crosstalk caused by sudden load current amplitude changes in the 220V domain due to the spatial density. Hence, in addition to certain chip partitioning issues, conceptual and constructive precautions have to be taken into account for SmartCoDe node system integration within a small sized package, accomplished e.g. by complete physical separation of 220V- and low voltage/RF-functions with additional ground-shielding in between.

Another aspect to be considered in system partitioning is the economic scalability of a SmartCode node. Due to the variety of possible applicative options (analogue/digital/no external interface, high/low/no security, routing node/only monitoring&control node,..), striving for single chip integration might not be the overall most cost-effective solution. Rather a scalable technology platform for heterogeneous, multi-chip integration with exchangeable and/or enrichable features looks like the better overall economic choice unless a single very high volume application case is found, justifying corresponding SoC-integration costs and risks. Options for heterogeneous system integration will be presented in chapter 4.

3.2 Semiconductor Technology Choice

There has been spending tremendous effort on the development of ever smaller feature-sized semiconductor technologies, known as deep sub-micron technologies or Nanotechnologies, with the target to let the area (costs) and power consumption shrink with every technology node and to squeeze out computation performance (also known as “More Moore”). However, shrinking of feature size also goes with a reduction of noise margin, particularly for analogue/mixed-signal functionality, due to the decrease of the core supply voltage. In order to provide reliable operation in the highly heterogeneous and challenging SmartCoDe environment, it is recommended and assumed to not use CMOS semiconductor technologies with a feature size smaller than 90-130nm.

3.3 Implementation of functions

For the digital/low-voltage functional modules

- Security Controller
- Application Controller
- RF Transceiver

(see also Figure 3) appropriate and "SiP-integration-friendly" off-the-shelf components are available (though there might be further optimization potential) as bare silicon dies, In addition they need only a few discrete passive components (crystal, inductors and capacitors for RF-antenna matching) for the implementation of the full functionality.

On the other hand there is no adequate (chip-) solution existing particularly for

- Power Metering
- Power Supply

for SmartCoDe system integration. One of the targets of the SmartCoDe consortium is to develop and design IC-prototypes for these functions, well suited for system integration, by reusing and adapting existing IP.

3.3.1 Power Metering

For performing power metering different options are available. All suitable options are based on separate voltage and current sensing with subsequent calculation of power- and energy figures by means of A/D conversion and digital filtering and post-processing.

Current Measurement

Some popular approaches have decisive drawbacks when used in the SmartCoDe scenario. As an example current measurement is often done by means of a shunt resistor. But as the load current to be measured always produces power losses in the shunt, scaling up with the amplitude of the load current, this would compromise the overall energy budget drastically, as the dominant power share would stem from the consumed shunt power.

In SmartCoDe a low power approach is targeted by measuring the load current through magnetic field measurements. This requires just a piece of special formed high voltage power line with a Hall sensor element precisely assembled in geometric relation to the power line. Further on the whole measurement circuitry can be integrated into a single die without the need of external components and will be assembled in highly isolated arrangement to the powerline

Voltage Measurement

Voltage measurements are anticipated by means of resistive or capacitive voltage dividing and subsequent A/D conversion. This functionality can be co-integrated into the Hall sensor chip. As a result the Power Measurement Unit can be designed by means of a single chip and a few small external components for voltage dividing.

3.3.2 Power Supply

The power supply is another crucial module of the SmartCoDe node, as if not providing proper efficiency this will lead to increased overall power consumption.

The Power Supply Module will consist of high efficiency AC/DC converters, transferring the 220V AC input into low voltage DC levels required by the SmartCoDe internal electronic circuits, with operation points well adapted to varying output currents. As most parts will be integrated into a CMOS silicon die, there will be only the need for a minimum number of external passive components.

4 Overview of Appropriate Assembly- and Packaging Technologies

In Chapter 3 it was shown that the implementation of the different SmartCoDe node internal functions can be accomplished and mapped to separate chips by the usage of different, well suited semiconductor technologies. This chapter now gives a short overview on appropriate assembly- and packaging technologies, suitable for heterogeneous system integration of a SmartCoDe node.

Figure 4 gives an overview on available backend technology platforms, scaling from simple leadframe and leadless packages for single chip integration, Wafer Level Packages (WLP) and finally embedded Wafer Level Packages (eWLB) with Fan Out solutions, which offers high-density ability for multi-chip system integration into a single package. Both laminate based packages and eWLB technology are suitable for SmartCoDe system integration, as they also optionally enable co-integration of passive components as well.

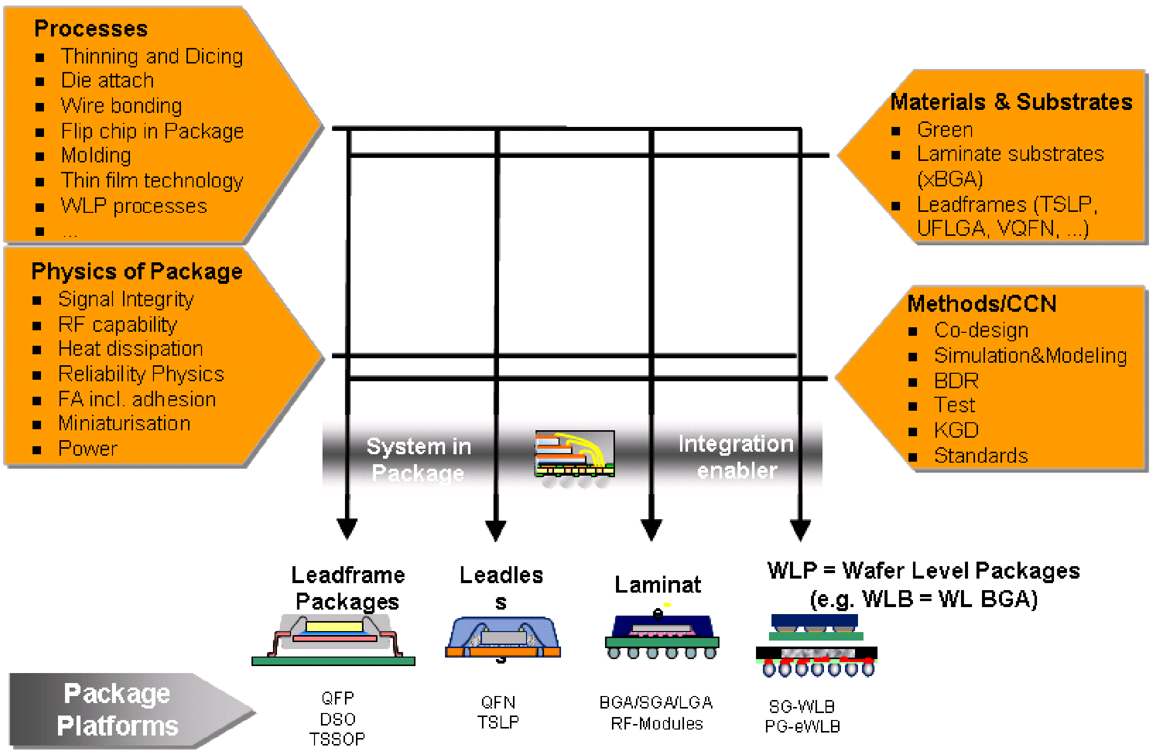

Figure 4: Packaging and Integration Enabling Assembly Technologies

Both laminate/PCB based and WLP based system integration is appropriate for SmartCoDe node integration. An overview of WLP technology is given in http://www.siliconfareast.com/wl_package.htm.

Unlike a PCB based approach, eWLB makes use of redistribution layers (multi-layer thin film metal rerouting) and bumps for the interconnection between components and external interfaces, thereby using the same deposition techniques as for device fabrication itself.

eWLB is particularly interesting as it paves the way towards a true integration of frontend- and backend-processes. It streamlines the manufacturing process undergone by a highly heterogeneously integrated device, like a SmartCoDe module, from silicon start over assembly, packaging, testing and shipment.

When using a PCB based approach both wire-bonding and flip-chip bonding can be used. But to keep assembly complexity and costs low it is recommended to rely on one certain assembly technology (either wire-bond or flip-chip). The chip protection can be done by the application of glob top, underfilling, casting or/and overmolding.

Making use of 3D-vertical stacking technologies is not recommended costwise. Side-by-side arrangement of components is the better choice unless unaccomplishable performance targets are the driving force for 3D-integration, which is not foreseen here.

5 SmartCoDe Node Cost Estimation

As a result of the assessment given in the previous chapters, the following cost estimation of a SmartCoDe HW node is based on certain assumptions:

- Certain minimum safety distance between external high voltage and signal pins
- Physical separation of high voltage and low voltage signal/RF modules
- Separate IC-components for Power Metering, Power supply, micro-controller, security controller and RF-transceiver
- Co-integration of passive devices (capacitors, inductors, crystal; all small sized SMD components) for voltage dividing, rectifying, RF-antenna matching, clock generation, blocking into the package
- Embedded Wafer level packaging or micro-PCB based carrier with cost-effective FR4 material with a small number of metal layers;
- No battery; system is supplied from 220V mains
- no need for 3D vertical stacking

Table 1 presents a first indicative cost estimation for a SmartCoDe HW-node broken down into manufacturing categories.

Topic	Cost	Share
BOM – Active Components	1.98 €	40.57 %
BOM –Discrete Passives	0.40 €	8.20 %
BOM - Substrate/Package	1.70 €	34.84 %
Assembly	0.80 €	16.39 %
Total costs for SmartCoDe HW node	**4.88 €**	**100 %**

Table 1: Cost estimation for a SmartCoDe HW node

The major cost share is given by the BOM, particularly the costs for active components and substrate/packaging sum up to 75% of the total costs. Figure 5 depicts the relations between different cost categories graphically.

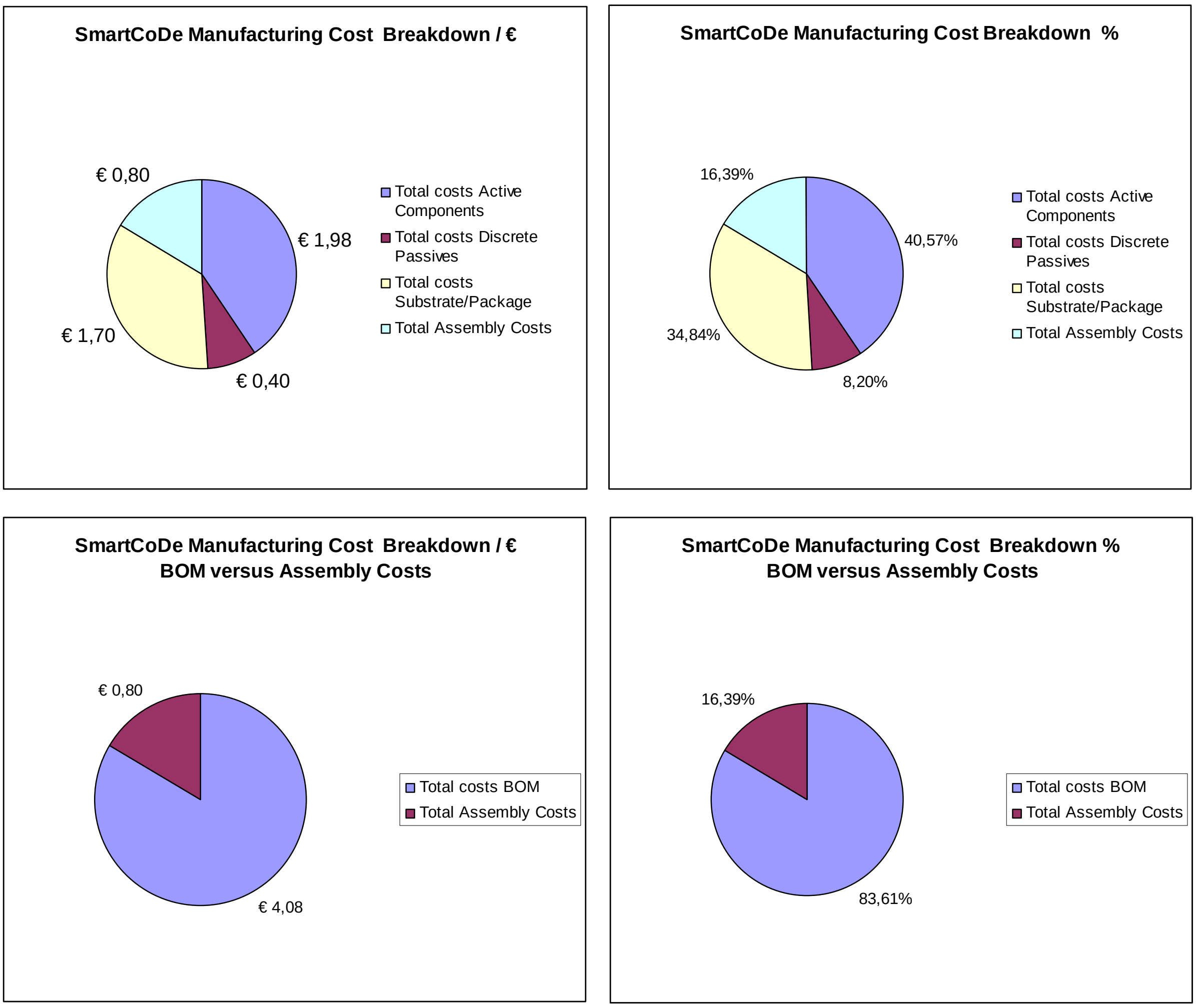

Figure 5: SmartCoDe Manufacturing Cost Breakdown

Table 1 and Figure 5 show first indicative figures. There is further potential for optimizations available:

- Higher SoC-integration, e.g. by the usage of integrating technologies, thereby reducing both silicon area and assembly complexity due to the reduced number of sub-components
- Reduction of discrete passives
- Taking product volume- and technology maturity aspects into account

As a further indicative figure,

6 Conclusion

As HW costs for Energy Management systems for homes and offices available on the market today are high, wide scale market penetration hasn't become reality by now.

With the upcoming smart power grid the availability of such systems at low prices becomes more and more stringent.

In order to close this gap this report showed first indicative HW cost figures, achievable by the consistent employment of miniaturization technologies offered by modern wafer fabs and backend technologies with its supporting heterogeneous integration capabilities. The estimation was based on an assessment of

- Required internal functions and functional requirements
- Certain partitioning into sub-components
- Employment of adequate System-in-Package assembly and packaging technologies allowing for high miniaturization
- Ability of co-integration of passive components
- Taking physical precautions into account

While these first indicative cost estimations are already very promising, further existing optimization potential has been highlighted.

7 Glossary

AC	Alternating Current
DC	Direct Current
EuP	Energy Using Products
HV	High Voltage
IP	Intellectual Property
PCB	Printed Circuit Board
RF	Radio Frequency
SiP	System in Package
SMD	Surface Mounted device
SoC	System on Chip
WLP/eWLB	Wafer Level Package/ Embedded Waferlevel Ball Grid Array

Table 2: Glossary