

SmartCoDe System-in-Package (SiP) Considerations



SmartCoDe Expert Cooperation Workshop Vienna/Austria 2011-10-12

Thomas Herndl (Presenter) – IFAT DCGR CRE Wolfgang Scherr - IFAT DC ATV SC D VI CE Mario Motz - IFAT DC ATV SC D VI INNO Josef Haid – IFAT DCGR CCS M Infineon Technologies Austria AG



Content

- > Introduction & Scope
- Status Development of Key Elements: Metering IC, Power Supply
- > Discussion on partitioning SiP/SoC
- > Conclusion





Introduction & Scope



FP7 ICT-2009

GA-No. 247473

3



Infineon Austria – Company Overview

Infineon Technologies Austria AG incl. subsidiaries





Environmental Sustainability at Infineon Enabling a Sustainable Society: Our Products

IFX provides products and solutions for the whole energy value chain





...Now Going Further to the Energy CONTROL Level

SmartCoDe Target Module

- Miniaturized wireless networked smart device for power metering and control of energy using products at low costs
 - Lighting units
 - (Home-) appliances
 - Intelligent power plug









Application cases to be considered

- > Lighting units (LED, neon lamps, halogen lamps, bulb, ...)
- Appliances control (e.g. fridge, washing machine, ..; with digital or analogue interface)
- > Intelligent power plug (Power plug control & metering)
- > Smart Metering only (measure, store and report metering information)
- > Sensors (temperature, humidity, presence, light level,...)
- Master- resp. Gateway Node (need to also perform SW-centric network management tasks, key management,...)

>





Basic Functional Blocks of a full functional SmartCoDe Node







Key Components developed throughout SmartCoDe







Key element: Current (Power) sensing



FP7 ICT-2009

GA-No. 247473





First functional Demonstrator (year 1)



A Constraints of the series of

Hall-based current sensor (analoque)

FPGA: dig. post-processing of current & voltage signals

BDA/DI DALI/DSI DA/D2 Test load: DALI controlled, dimmable halogen transformer

C N418 V99





TRIDONIC.ATCO TE-0150 one4all sc

Digital diminable safety isolating 230-240//121/150VA 0/50/90H

switchDIM



Noise & Dynamic Range of Current Sensor Section

typical & target values







FP7 ICT-2009

Power Supply





SmartCoDe Power Supply SMPS based, with detector and capacitive startup



- No clumsy components
- Low count of external passives
- High efficiency



FP7 ICT-2009

Development ongoing



Discussion: Partitioning SiP/SoC



FP7 ICT-2009

GA-No. 247473



SoC or SiP ?

> SoC:



- Integrating CMOS technologies can implement almost all functions on single chip, with some external passives
- > Optimize chip-area, reduce assembly- and logistic costs
- > Pays off only for highest volume
- > Could be long term target once standardizing issues are clearly settled
- SiP:
 - Can use different, "best fitting" semiconductor technologies and specific process optimizations
 - > Due to low number of component-I/Os and interconnects in a SmartCoDe node this does not add significant costs:
 - no multi-layer substrates/PCBs required
 - Could apply cheap sub-packaging
 - » e.g. SMD only to make use of homogeneous assembly line
 - » cope with heterogeneous reliability/hermeticity requirements
 - low risk of yield drop
 - > Mid-term target: chip embedding/eWLP => keep value chain in wafer fab
 - paves the way towards a true integration of frontend- and backend-processes.
 It streamlines the manufacturing process undergone by a highly
 heterogeneously integrated device, like a SmartCoDe module, from silicon
 start over assembly, packaging, testing and shipment.



SmartCoDe Partitioning Option 1







SmartCoDe Partitioning Option 2



Smart DeExample of a "minimum" system configuration:Smart DeLED Lamp control



 \Rightarrow not all applications might require all functional units

iSM for MAC-acceleration & simple protocols/applications

 \Rightarrow due to the high number of light sources in buildings a highly optimized approach is particularly interesting



21



Initial SmartCoDe HW Node Cost Indications

SmartCoDe Manufacturing Cost Breakdown %



- Total costs: < 5€ possible (based on full functional node)
- Lower costs possible if not all functions are required or when striving for higher single chip integration (costs are BOM dominated)





Possible Cost Optimizations

- > Costs dominated by
 - active components
 - substrate/packaging
- > Means for Optimization
 - cost drop over the years
 - particularly for eWLP once mature, homogeneous Frontend/Backend fabs are set in place
 - higher single chip integration (of heterogeneous functions; e.g. usage of CMOS integration technologies)
 - tailoring/optimization to specific (killer-niche) application
 - digitally intensive approaches (digital logic shrinks best)
 - different feature variants (w/wo security, power supply, metering)







An affordable technology for everyone...



Tent lights off !

Thank you for your attention...

Never stop thinking

